CLAIMS

1. A digital baseband circuit, comprising:

   first and second input ports for receiving digital input signals;

   a controller coupled to the first and second input for estimating the gain and phase imbalance of the digital input signals.

2. A digital baseband circuit as defined in claim 1, wherein the controller estimates the gain mismatch as:

   $\hat{\gamma} = \frac{g_I}{g_Q} = \frac{\alpha_I - \beta_Q}{\alpha_I + \beta_Q}$, where g_I, g_Q are the gains of the real and imaginary components of the digital input signals, α_i is a pilot symbol despread by a normal spreading sequence and is the pilot symbol despread by a IQ-swapped spreading sequence.

3. A digital baseband circuit as defined in claim 1, wherein the controller comprises a digital signal processor.

4. A digital baseband circuit as defined in claim 2, wherein the controller estimates the phase mismatch as:

$$\hat{\theta} = 2\tan^{-1}\frac{\alpha_Q - \beta_I}{\alpha_I - \beta_Q} = -2\tan^{-1}\frac{\alpha_Q + \beta_I}{\alpha_I + \beta_Q},$$

wherein α_I and $\alpha_Q$are pilot symbols despread by a normal spreading sequence and β_I and β_Q are pilot symbols despread by an I/Q-swapped spreading sequence.

5. A digital baseband circuit as defined in claim 2, further comprising:

a gain and phase correction circuit coupled to the first and second input ports.

6. A digital baseband circuit as defined in claim 5, wherein the gain and phase correction circuit includes first and second multipliers coupled to the first input port and third and fourth multipliers coupled to the second input port.

7. A digital baseband circuit as defined in claim 6, wherein the gain and phase correction circuit further comprises a look-up-table coupled to the first, second, third and fourth multipliers.

8. A digital baseband circuit as defined in claim 7, wherein the look-up-table comprises a read-only memory (ROM).

9. A digital baseband circuit as defined in claim 5, wherein the controller estimates the phase mismatch as:

$$\hat{\theta} = 2\tan^{-1}\frac{\alpha_Q - \beta_I}{\alpha_I - \beta_Q},$$

wherein α_I and α_Q are pilot symbols despread by a normal spreading sequence and β_I and β_Q are pilot symbols despread by an I/Q-swapped spreading sequence; and

the gain and phase correction circuit uses phase and gain estimates to provide a gain and phase correction to the digital input signals.

10. A digital baseband circuit as defined in claim 9, wherein the gain and phase correction circuit applies correction to the digital input signals using the formula:

$$X(\gamma,\theta) = \frac{1/g_Q}{\cos(\theta/2)+\sin(\theta/2)}\begin{bmatrix}\dfrac{\cos(\theta/2)}{\gamma} & \sin(\theta/2)\\ \dfrac{\sin(\theta/2)}{\gamma} & \cos(\theta/2)\end{bmatrix}.$$

11. A method for estimating and correcting the gain and phase imbalance of digital signals in a direct sequence code division multiple access (DS-CDMA) system, comprising the steps of:

estimating the gain imbalance as follows:

$\hat{\gamma} = \frac{g_I}{g_Q} = \frac{\alpha_I - \beta_Q}{\alpha_I + \beta_Q}$, where g_I, g_Q are the gains of the real and imaginary components of the digital input signals, α_I is a pilot symbol despread by a normal spreading sequence and β_Q is the pilot symbol despread by a I/Q-swapped spreading sequence; and

estimating the phase imbalance as follows:

$\hat{\theta} = 2\tan^{-1}\frac{\alpha_Q - \beta_I}{\alpha_I - \beta_Q}$, where α_I and α_Q are pilot symbols despread by a normal spreading sequence and β_I and β_Q are pilot symbols despread by an I/Q-swapped spreading sequence.

12. A method as defined in claim 11, further comprising the step of:

using the gain and phase imbalance estimates to correct for the gain and phase imbalance in the digital signals, using the formula:

$$X(\gamma,\theta)=\frac{1/g_Q}{\cos(\theta/2)+\sin(\theta/2)}\begin{bmatrix}\dfrac{\cos(\theta/2)}{\gamma} & \sin(\theta/2)\\ \dfrac{\sin(\theta/2)}{\gamma} & \cos(\theta/2)\end{bmatrix}.$$

13. A method as defined in claim 12, wherein the correction of the gain and phase is performed by a gain and phase correction circuit having a plurality of multipliers, and a look-up-table providing the plurality of multipliers gain and phase offset correction information based on gain and phase imbalance information.

14. A method of estimating the amplitude mismatch (gain imbalance) in a Code Division Multiple Access (CDMA) receiver, comprising the steps of:

(a) determining the real component of a pilot signal by a normal spreading sequence;

(b) determining the imaginary component of the pilot signal despread by an IQ-swapped spreading sequence; and

(c) finding the difference between the real component of the despread pilot signal and the imaginary component of the IQ-swapped pilot signal.

15. A method as defined in claim 14, wherein steps (a) and (b) are performed by a correlator.

16. A method as defined in claim 15, wherein step (c) is performed by a digital signal processor.

17. A method of estimating the phase mismatch (phase imbalance) in a Code Division Multiple Access (CDMA) receiver, comprising the steps of:

(a) determining the imaginary component of a pilot signal despread by a spreading sequence;

(b) determining the real component of the pilot signal despread by an IQ-swapped spreading sequence; and

(d) finding the difference between the imaginary component of the regular despread pilot signal and the real component of the IQ-swapped pilot signal.

18. A method as defined in claim 17, wherein steps (a) and (b) are performed by a correlator.

19. A method as defined in claim 18, wherein step (c) is performed by a digital signal processor.

20. A gain and phase correction circuit, comprising:

a first input port for receiving an inphase (I) digital signal;

a second input port for receiving a quadrature (Q) phase signal;

first, second, third and fourth multipliers, the first and third multipliers having first input ports for receiving the I signal and the second and fourth multipliers having first input ports for receiving the Q signal; and

a memory device having first, second, third and fourth output ports, said first output port coupled to a second input port of the first multiplier, said second output port coupled to a second input port of the second multiplier, said third output port coupled to a second input port in the third multiplier, and said fourth output port coupled to a second input port in the fourth multiplier, said memory device having a first input port for receiving a gain imbalance estimate, and a second input port for receiving a phase imbalance input port.

21. A gain and phase correction circuit as defined in claim 20, wherein the memory device comprises a read-only memory (ROM).

22. A gain and phase correction circuit as defined in claim 20, further comprising:

a fifth multiplier having a first input port for receiving an output from said first multiplier and a second input port for receiving an output from said second multiplier, and having an output port for providing a corrected I signal; and

a sixth multiplier having a first input port for receiving an output from said third multiplier and a second input port for receiving an output from said fourth multiplier, and having an output port for providing a corrected Q signal.

23. A gain and phase correction circuit as defined in claim 20, wherein the I and Q signals are digital signals.